Measurement-Based Large-Signal Diode Modeling System for Circuit and Device Design

David E. Root, *Member, IEEE,* Marco Pirola, Siqi Fan, William J. Anklam, *Member, IEEE,* and Alex Cognata

***Abstract*—A new relaxation-time large-signal table-based diode model for circuit simulation and an associated automated system which characterizes the device and generates the model data file, are presented. Excellent agreement between simulated and measured fundamental and second through fourth harmonic power levels is demonstrated for a HEMT diode up to frequencies of 48 GHz. Excellent agreement is demonstrated between simulated and measured large-signal oscillation frequency versus varactor tuning voltage for a varactor-tuned oscillator circuit fabricated with a varactor diode designed using the model.**

Introduction

HETEROSTRUCTURE and varactor diodes have charge–voltage relations and current–voltage relations under reverse bias and breakdown conditions that can be quite different from the simplified explicit formulas used by most large-signal models [8]. For example, the depletion layer capacitance of an ideal diode is given in (1), where C_{j0} is the zero bias capacitance, ϕ is the barrier height, and γ is the grading coefficient. Equation (1) is only applicable to real varactor diodes over small ranges of bias and, in general, γ must be considered to be voltage dependent. Better fits to capacitance data over a wider range of bias can be obtained using more complicated empirical expressions for which an equation-specific parameter extraction methodology must also be developed [10].

$$C_j(V) = \frac{C_{j0}}{\left(1 - \frac{V}{\phi}\right)^{\gamma}} \tag{1}$$

In contrast, the modeling approach described in this paper defines the intrinsic nonlinear current–voltage and charge–voltage constitutive relations by means of appropriate spline interpolation of several bias-dependent functions computed directly from the measured dc and small-signal S-parameter data as functions of bias. This ensures both excellent model accuracy and great flexibility by making the model largely independent of the device process and technology; the model generation procedure is the same for any device for which the dynamical equations ("equivalent circuit") is valid, independent of the functional form of the constitutive relations. This technique, applied originally to GaAs MESFET and HEMT transistors [1], has been successfully applied to GaAs MESFET and MODFET (HEMT) diodes, and varactor diodes in one- or two-port configurations. The automated system presented here adaptively characterizes the diode over its entire safe operating range, taking more data where needed depending on the local nonlinearities of the DUT. The model generator constructs a complete large-signal model from the data, including parasitic extrinsic element values and bias-dependent functions from which device-specific nonlinear current–voltage and charge–voltage model constitutive relations are defined. Spline functions interpolate the tabulated nonlinear model functions during simulations. The validity of the model is confirmed herein by comparisons of simulations to measured dc data, small-signal S-parameter data versus bias and frequency, and extensive large-scale measurements of gain and harmonic levels versus output power at several bias points and different fundamental frequencies.

Another novel feature of this work is the use of the table-based model *before* device fabrication as a key component in a process of customized *device design*. Meeting the performance specifications of varactor-tuned oscillators [5] and nonlinear transmission lines [6], for example, requires the development of varactor diodes with customized C–V characteristics. In particular, the varactor C–V characteristic has a direct impact on the tuning range and tuning linearity of varactor oscillators and on the voltage-dependent delay and pulse steepening performance of nonlinear transmission lines. By using a table-based model for the varactor capacitance, the device or circuit designer can accurately specify a C–V characteristic without having to explicitly generate a closed-form nonlinear C–V equation for each desired variation. The ease with which a table-based C–V model can be generated allows the designer to investigate a wide range of C–V characteristics. Once the circuit simulations meet specifications, a doping profile can be extracted from the successful C–V characteristic. At this point epitaxial layer growth or implant schedules can be designed to produce wafers on which the circuits can be fabricated and tested. This procedure is verified by comparing simulations and measurements of a varactor-tuned oscillator circuit fabricated with a GaAs

Manuscript received March 26, 1993; revised June 15, 1993.

D. E. Root, W. J. Anklam, and A. Cognata are with Hewlett Packard Company, Microwave Technology Division, Santa Rosa, CA 95403.

M. Pirola is with the Dipartimento di Elettronica, Politecnico di Torino, Torino, Italy.

S. Fan is with the Hewlett Packard Company, Santa Rosa Systems Division, Santa Rosa, CA 95403.

IEEE Log Number 9213006.

varactor diode, the epitaxial structure of which was designed using the model.

The Model

Fig. 1 illustrates a standard equivalent circuit model for the diode. Interpreted as a linearized model at each intrinsic bias voltage V, the intrinsic admittance, Y_a, is expressed by (2a). There are three bias-dependent functions $G_{DC}(V)$, $R(V)$, and $C(V)$, which must be independently specified. Interpreted as a large-signal model composed of a two-terminal voltage-dependent resistor in series with a voltage-dependent capacitor, all in parallel with a voltage-controlled current source, the linearized admittance takes the form of (2b). This time, there are only *two* bias-dependent functions, $G_{DC}(V)$, and $C(V)$, which must be independently specified. The reason is that no voltage is dropped across the two-terminal nonlinear resistor in series with the capacitor under any dc bias. Therefore, whatever its constitutive relation, its resistance will always (in small-signal at least) be its value with no voltage across it.

$$Y_a(V, \omega) = \frac{j\omega C(V)}{1 + j\omega R(V) C(V)} + G_{DC}(V) \qquad (2a)$$

$$Y_b(V, \omega) = \frac{j\omega C(V)}{1 + j\omega R(0) C(V)} + G_{DC}(V). \qquad (2b)$$

If the large-signal model is to reduce to the bias-dependent admittance of (2a), either more circuit elements or else more complicated elements must be used. The solution adopted in this work is to express the dynamical equation of the model in terms of an implicit ordinary differential equation for the instantaneous current, which has bias-dependent coefficients related to the three independent bias-dependent functions of (2a). In particular, a first-order differential equation, or relaxation-time equation [2], is used which is similar in form to those reported recently for nonquasi-static FET models [1], [2], [7]. The three independent constitutive relations which must be specified are the stored charge, $Q(V)$, related to $C(V)$ by simple integration, $I_{DC}(V)$, similarly related to $G_{DC}(V)$, and the relaxation time $\tau(V)$, given by the product of $C(V)$ and $R(V)$. The implementation of the model is such that it can be used for large-signal transient analysis in the time-domain, large-signal harmonic balance in the frequency domain, small-signal analysis in the frequency domain, and many other analysis types.

Automated Measurement-Based Modeling System

The interpolation of the bias-dependent model functions, with respect to the intrinsic voltage, and the sampling of the device data in bias space are both critical for the correct model behavior. Naive interpolation and improper sampling rates can result in spline oscillations between discrete data points, and can cause convergence problems for the harmonic balance and transient analysis

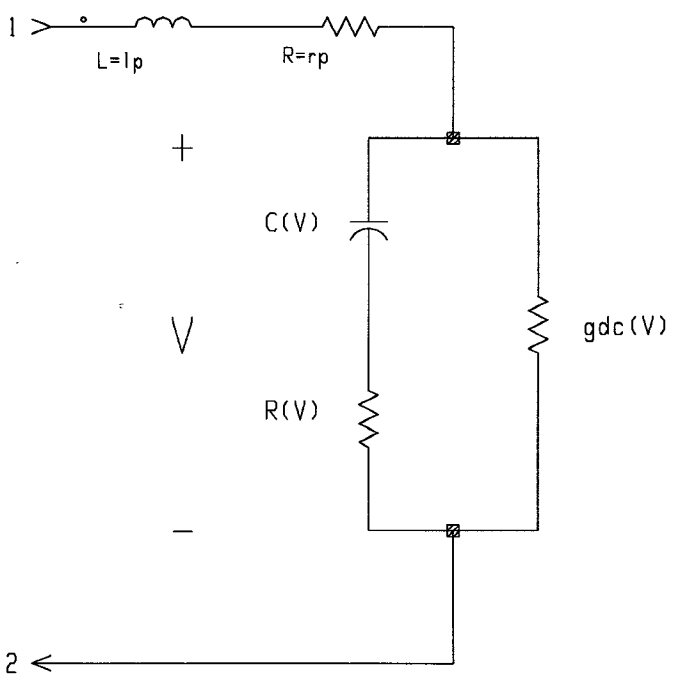


Fig. 1. Equivalent circuit of a general diode. Interpreted as a linear circuit at each bias, the element values are parameterized by the dc bias, V, applied to the device (neglecting the voltage drop across the parasitic resistance for simplicity). This corresponds to an admittance function for the intrinsic device given by (2a). As explained in the text, one cannot construct a large-signal model by replacing the three bias-dependent linearized elements by a two-terminal nonlinear capacitor and a pair of two-terminal nonlinear resistors and still obtain the same bias-dependent admittance as (2a). The large-signal model described in this paper implements a relaxation-time differential equation for the terminal current with three bias-dependent coefficients which are related to the parameterized linear element values.

algorithms. To minimize these problems, as well as to save measurement time and data storage requirements, the bias points are adaptively computed by the automated system using a predictor corrector algorithm [1] based upon the device-specific dc current and intrinsic capacitance versus bias behavior. In addition, the simulator performs spline interpolation on functions of the data [e.g., Log (I)], rather than interpolating the data directly. This technique provides better extrapolation beyond the boundary of the measured data than obtained by extrapolating the data directly. Fig. 2 shows a comparison of a subset of the current–voltage relation between measured (discrete triangles), the new model (well-behaved curve) and a direct application of a cubic spline-interpolation (nonmonotonic curve) of the measured current.

The automated data acquisition and model generator system is based on the HP 85122A parameter extraction test system, consisting of an HP 8510 network analyzer and HP 4142DC source/monitor, with software implemented in the HP ICCAP program for measurement control and graphical interface. DC and single-frequency S-parameters are taken over the entire safe operating region of the device. The extrinsic parameters are extracted by means of single frequency small signal measurements with the device forward biased [3]. The link between the automated data acquisition/model generator system and

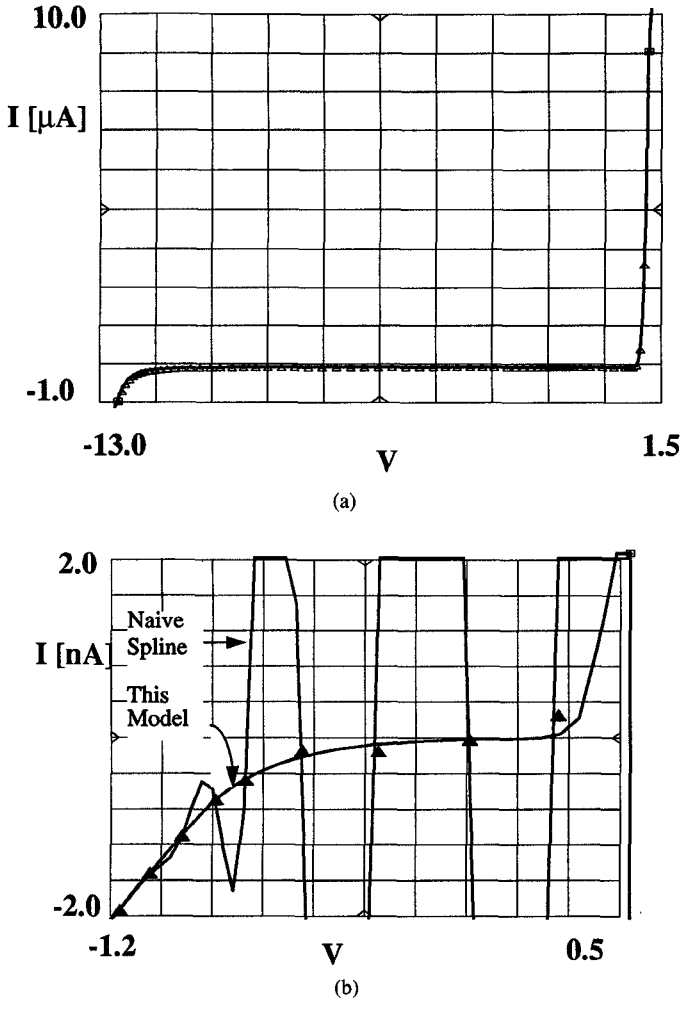


Fig. 2. Measured (▲), modeled (well-behaved solid lines), and naive spline-interpolated (wavy solid lines) dc I–V relations for a MODFET Diode. (a) From breakdown to full forward bias. The model is well-behaved over the entire range of device operation. Oscillations of a simple piece-wise cubic spline interpolation are not visible at this scale. (b) Magnified scale near zero current. The model is well-behaved and goes through all the data points except when the measured current is in the noise level (500 pA in this case). The oscillations of the naive splines are clearly visible at this scale.

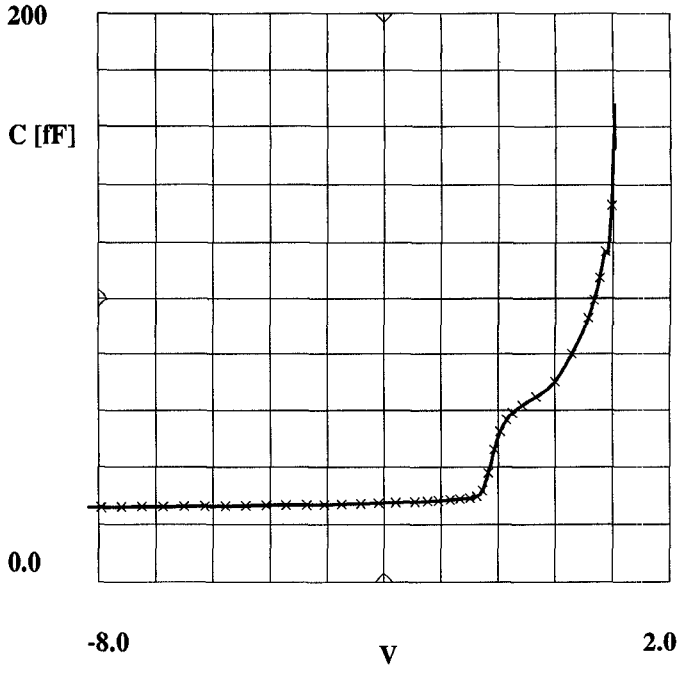


Fig. 3. Measured (×) and modeled (——) C–V relation for MODFET diode. The agreement with data is much better than that which can be obtained by fitting to fixed, "canned" model constitutive relations based on simplified physics or empirical expressions.

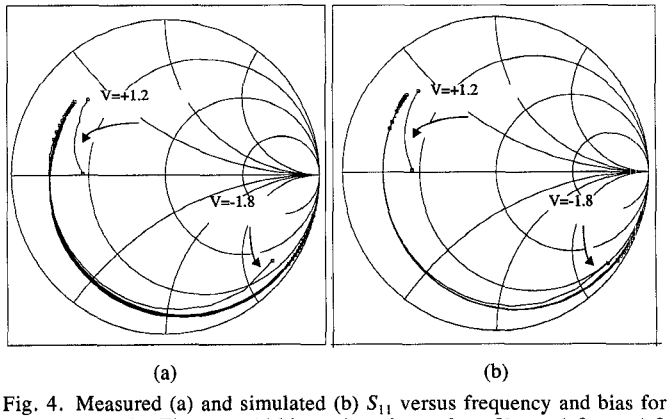


Fig. 4. Measured (a) and simulated (b) S_{11} versus frequency and bias for a varactor diode. There are 14 bias points shown from $V = -1.8$ to $+1.2$ V. The frequencies range from 1 to 26 GHz. Recall the model was constructed from data at the *single* frequency of 3 GHz.

the simulator is accomplished by the model data file containing the parasitic element values and the dc and other intrinsic model functions of the internal bias. This file, containing the device characterization, is the only input required by the simulator.

Fig. 3 compares measured (×) and modeled (——) C–V nonlinear constitutive relations for a MODFET diode. The modeled curves are nearly identical to the measurements.

Fig. 4 compares measured (a) and simulated (b) S_{11} versus bias and frequency for a varactor diode. Fourteen bias points are compared from $V = -1.8$ to $V = +1.2$ V. The frequency range is 1–26 GHz. For each bias point, the agreement between simulations and measurements is very good over the entire frequency range, despite the fact that the model data file was constructed from S-parameters measured at the *single frequency* of 3 GHz.

Large-Signal HEMT Diode Verification

Fig. 5(a) and (b) compares simulated (solid lines) to measured large-signal gain (▲) in dB, and second harmonic (·), third harmonic (+), and fourth harmonic (×) levels in dBc versus output power for a 48 μm two-port MODFET diode. The bias for this comparison is $V = -0.5$ V, and the fundamental frequency is 2 GHz. The agreement is excellent.

Fig. 6(a) and (b) compares simulations and measurements under the same conditions as Fig. 5, except now the diode is forward-biased to +0.5 V. Again, the agreement is excellent, except perhaps for the fourth harmonic at very low power levels, where the large-signal measurement is questionable. The model even predicts the mea-

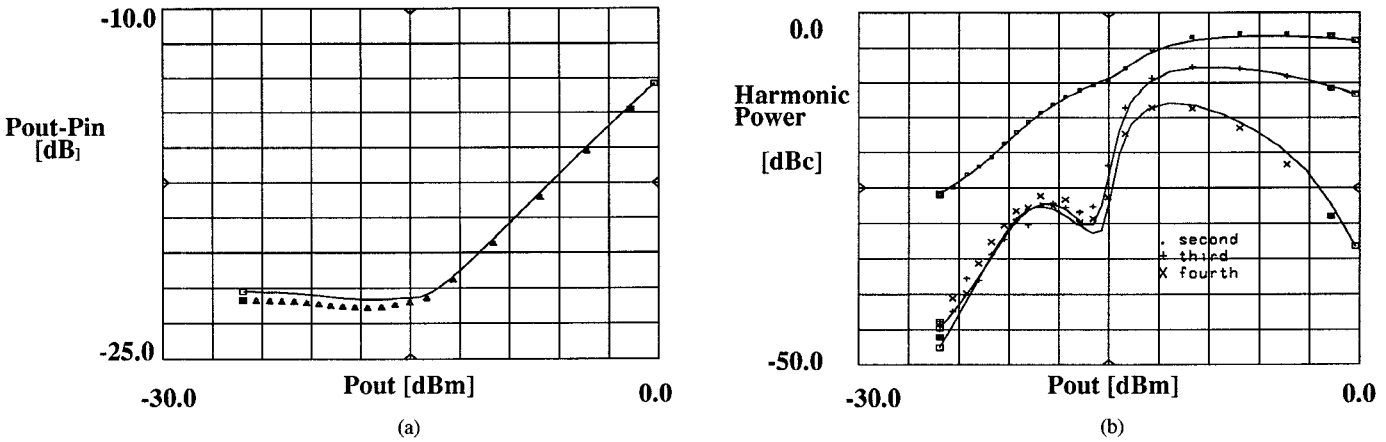


Fig. 5. Simulated (solid lines) and measured gain (▲), second harmonic levels (·), third harmonic levels (+), and fourth harmonic levels (×) versus output power for a MODFET diode. Bias: $V = -0.5$. Fundamental frequency 2 GHz.

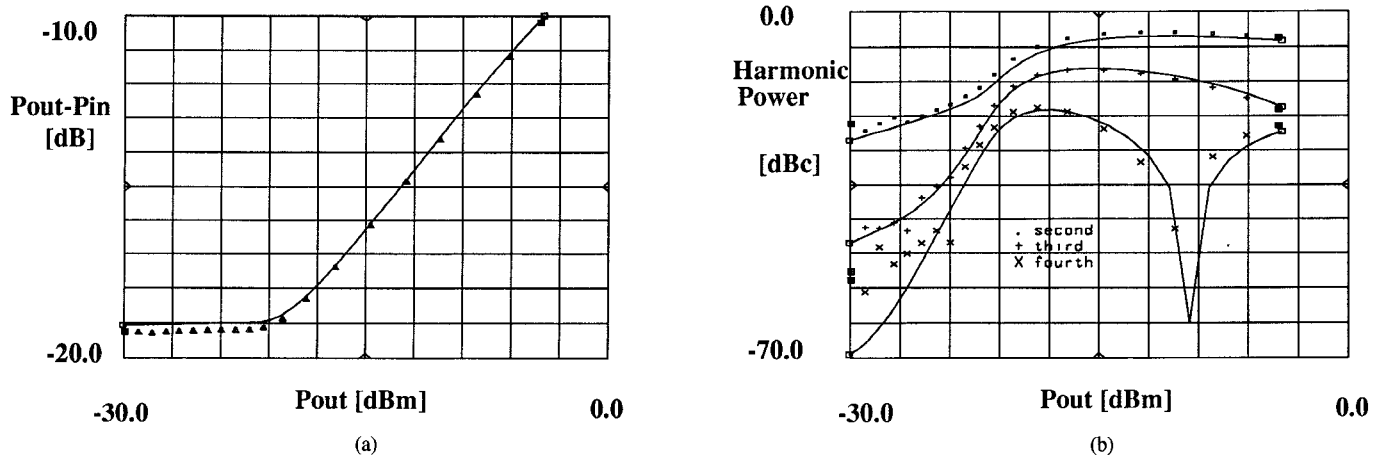


Fig. 6. Simulated (solid lines) and measured gain (▲), second harmonic levels (·), third harmonic levels (+), and fourth harmonic levels (×) versus output power for a MODFET diode. Bias: $V = +0.5$. Fundamental frequency 2 GHz.

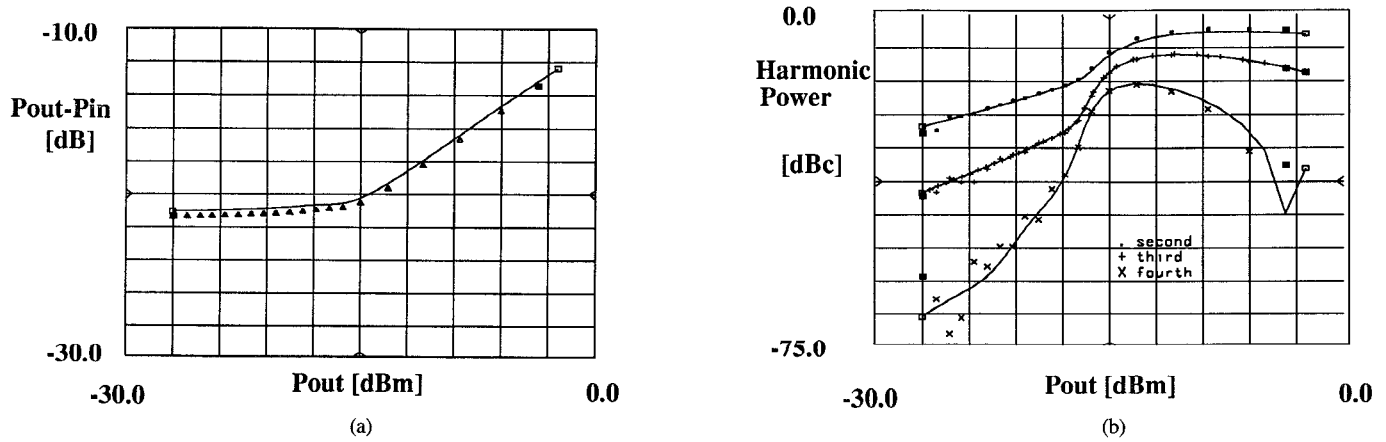


Fig. 7. Simulated (solid lines) and measured gain (▲), second harmonic levels (·), third harmonic levels (+), and fourth harmonic levels (×) versus output power for a MODFET diode. Bias: $V = 0$. Fundamental frequency 2 GHz.

sured sharp depression in the fourth harmonic at about Pout $= -10$ dBm.

Fig. 7(a) and (b) compares simulations and measurements under the same conditions as Fig. 6, except now the diode is unbiased ($V = 0.0$ V). The fundamental frequency is 2 GHz. The agreement is excellent except perhaps for the fourth harmonic at very low power levels, where the large-signal measurement accuracy is questionable.

Fig. 8(a) and (b) compares simulations and measure-

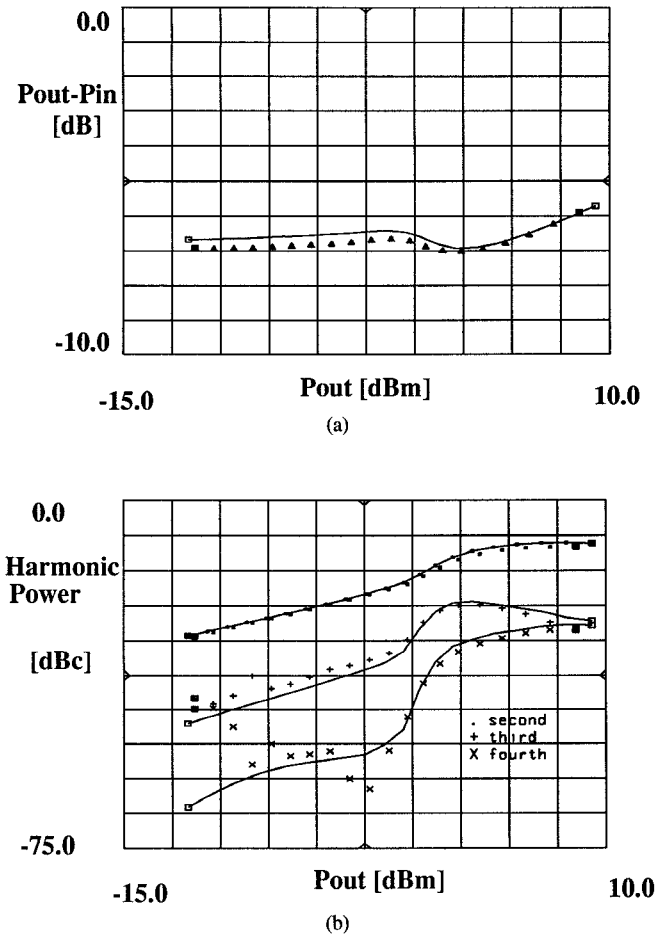


Fig. 8. Simulated (solid lines) and measured gain (▲), second harmonic levels (·), third harmonic levels (+), and fourth harmonic levels (×) versus output power for a MODFET diode. Bias: $V = 0$. Fundamental frequency 12 GHz.

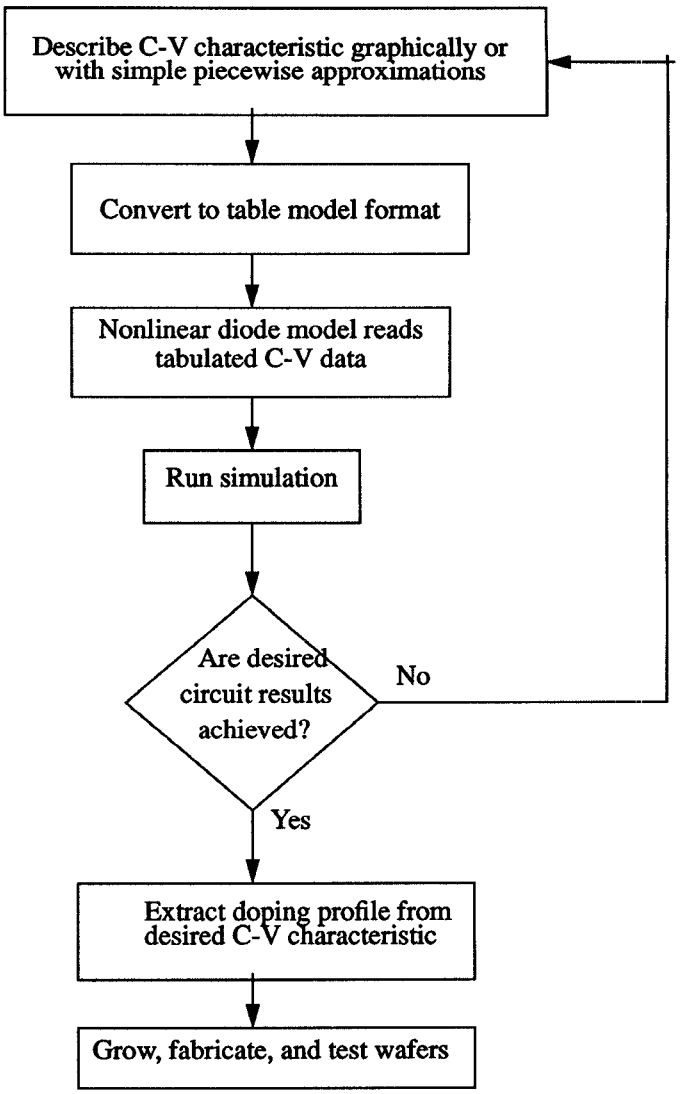


Fig. 9. Flow chart depicting the use of the nonlinear table-based diode model in the design of the varactor diode epitaxial structure for a given nonlinear circuit performance goal.

ments under the same conditions as Fig. 7, except now the fundamental frequency for the measurements and simulations is 12 GHz. Again, the agreement is excellent. This proves that the model, also extracted at the single frequency of 3 GHz, accurately predicts large-signal performance of this device up to at least 48 GHz, which is the frequency of the fourth harmonic with respect to the 12 GHz fundamental.

The large-signal data were measured using the on-wafer power and harmonic measurement system reported in [4]. The system provides on-wafer, vector error-corrected power and harmonic levels and large-signal reflection coefficient.

Varactor Device Design and Verification Using Varactor-Tuned Oscillator Circuit

Fig. 9 shows a flowchart of how the table-based nonlinear model is used in the customized device design process. The first step is to describe the trial C–V relation graphically or with simple piecewise approximations. Next, discretized values are read into the diode model "data file" tables. A large-signal simulation is done next. The model reads and interpolates the specified nonlinear constitutive relations during the simulation. If the desired circuit results are not achieved, the trial C–V relation is modified and the process iterated. When the desired circuit results are achieved, a doping profile is extracted from the successful C–V characteristic. At this point, epitaxial layer growth or implant schedules are designed to produce wafers on which the circuits can be fabricated and tested.

The fruitfulness of this approach was demonstrated by using the above procedure to design the epitaxial structure of a GaAs varactor diode and a varactor-tuned oscillator circuit. Fig. 10(a) depicts a simplified schematic of the varactor-tuned oscillator circuit. A large-signal oscillator analysis was performed with the HP MNS harmonic balance simulator [9]. The measured and simulated large-signal oscillation frequency versus tuning voltage is presented in Fig. 10(b), showing agreement within 3 percent over the entire tuning range. The measured circuit performance met its design goals of frequency linearity with tuning voltage and tuning range over the frequency band.

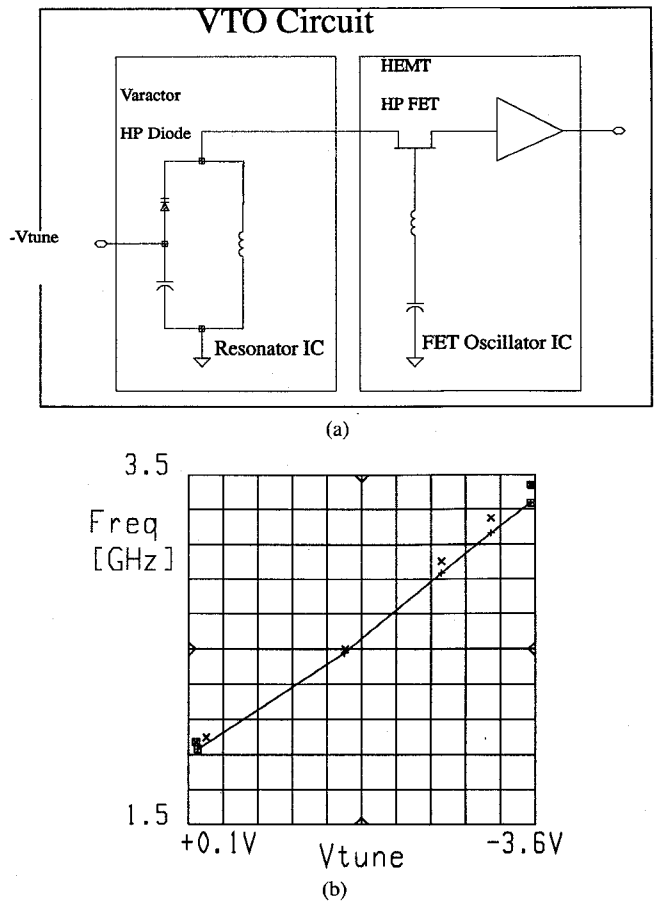


Fig. 10. Varactor-tuned oscillator circuit composed of FET oscillator IC and resonator IC containing a custom-designed varactor diode. (b) measured (×) and simulated (+) large-signal oscillation frequency versus tuning voltage for the varactor-tuned oscillator circuit of (a).

It should be noted that the FET active device model used for the FET Oscillator IC is the nonquasi-static measurement-based MESFET/HEMT model reported in [1].

Conclusions

The results and methodology presented above prove the measurement-based large-signal diode model and its associated automated data acquisition and model generator system yield accurate simulations of diode devices from diverse technologies over a wide variety of biases, frequencies, and input signal amplitudes. This demonstrates the measurement-based modeling system to be a valid CAD tool for automated diode characterization and for large and small-signal analysis and design of circuits and systems where such devices are key components. Moreover, the ease with which the model tables can be specified by device designers makes the model an important tool in the design of active diodes requiring customized nonlinearities for specific large-signal circuit applications.

Acknowledgment

The authors thank D. Albin for providing varactor-tuned oscillator data and simulation results, Dr. T. Parker for a helpful technical discussion, Dr. B. Hughes for reviewing the manuscript, K. Kerwin for technical suggestions and figure assistance, and Hewlett-Packard Management for supporting this work.

References

[1] D. E. Root, S. Fan, and J. Meyer, "Technology independent non quasi-static FET models by direct construction from automatically characterized device data," in *21st Euro. Microwave Conf. Proc.*, Stuttgart, Germany, Sept. 1991, pp. 927–932.

[2] M. C. Foisy, P. E. Jeroma, and G. H. Martin, "Large signal relaxation-time model for HEMTs and MESFETs," in *1992 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 251–254.

[3] B. Hughes and P. J. Tasker, "Bias dependence of the MODFET intrinsic model element values at microwave frequencies," *IEEE Trans. Electron Dev.*, ED-36, pp. 2267–2273, 1989.

[4] B. Hughes, A. Ferrero, and A. Cognata, "Accurate on-wafer power and harmonic measurements of MM-wave amplifiers and devices," in *1992 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1019–1022.

[5] P. J. McNally, *et al.*, "Ku and K-band GaAs MMIC varactor-tuned FET oscillators using MEV ion-implanted buried-layer back contacts," in *1990 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 189–193.

[6] W. Whiteley, W. E. Kunz, and W. J. Anklam, "50 GHz sampler hybrid utilizing a small shockline and an internal SRD," in *1991 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 895–898.

[7] P. Roblin, S. C. Kang, and W. R. Liou, "Improved small-signal equivalent circuit model and large-signal state equations for the MOSFET/MODFET wave equation," *IEEE Trans. Electron. Dev.*, vol. ED-38, p. 1706, 1991.

[8] P. Antognetti and G. Massobrio, Eds., *Semiconductor Device Modeling with SPICE*. New York: McGraw-Hill, 1988.

[9] HP85150B Microwave Design System: Discovering the System: Building and Analyzing Circuits, vol. 2. Ch. 13, pp. 2–19. Part 85150-90042.

[10] V. I. Cojocaru and T. J. Brazil, "A large-signal equivalent circuit model for hyperabrupt *p–n* junction varactor diodes," in *22nd Euro. Microwave Conf. Proc.*, vol. 2, Espoo, Finland, 1992.

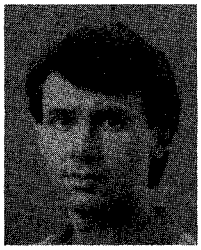
David E. Root (M'90) received the B.S. degree in physics, the B.S. degree in mathematics, and the Ph.D. degree in (theoretical) physics in 1986, all from M.I.T., Cambridge, MA.

In 1985 he joined Hewlett-Packard's Microwave Technology Division, Santa Rosa, CA, as a member of the R&D Technical Staff where he developed the first charge-based active-capacitance large-signal GaAs MESFET model for SPICE in 1987. Much of his recent work has focused on technology-independent large-signal modeling based on adaptive bias-dependent measurements. He was the originator and a principal technical contributor to the HP Measurement-Based Large-Signal FET Model, Model-Generator, and Automated Data Acquisition System, announced in 1991. He has published numerous papers and articles on nonlinear FET modeling, and presented many technical lectures around the world at both universities and industries. He is currently a Research and Development Scientist working in the general areas of active semiconductor device modeling for circuit simulation and CAE.

Marco Pirola, photograph and biography not available at the time of publication.

Siqi Fan was born in Beijing, China, in 1959. He received the Bachelor's degree in physics from Nanjing University in 1982, and the M.S. degrees in physics and electrical engineering from the University of Wisconsin-Milwaukee in 1988 and 1990, respectively.

From 1983 to 1986 he was employed at the Institute of Acoustics, Academia Sinica, Beijing. He has been with Hewlett Packard Company's Santa Rosa Systems Division CAE group as a Project Engineer since 1990. He was a principal technical contributor to the HP Measurement-Based Large-Signal FET Model, Model-Generator, and Automated Data Acquisition System. His interests include high-frequency semiconductor device modeling, nondestructive testing, and other applications of microwaves.



William J. Anklam (S'82–M'86) received the B.Sc. degree in electrical engineering from Iowa State University, Ames, in 1982 and the M.Sc. and Engineer degrees in electrical engineering from Stanford University, Stanford, CA, in 1983 and 1986, respectively.

He was a Research Assistant at the Ginzton Laboratory, Stanford University, from 1982 to 1985, investigating the fabrication and microwave properties of Josephson SNS microbridge series arrays. In 1985 he joined the Hewlett-Packard Microwave Technology Division, Santa Rosa, CA, where he was responsible for the design and characterization of planar-doped barrier diodes, Schottky diodes, and hyperabrupt varactors for microwave and millimeter-wave instrumentation as well as nonlinear transmission lines for high-speed sampling oscilloscopes. He is currently involved in the design of GaAs MMIC's with applications to lightwave and digital test systems.

Alex Cognata received the Associate of Science degree in electronic technology from Santa Rosa Junior College in 1983.

He is presently a Microwave Measurement Technician at the Hewlett Packard Microwave Technology Division, Santa Rosa, CA. He has co-developed a noise parameter measurement system and, more recently, co-developed a vector-corrected 0.5–50 GHz Harmonic Loadpull system. With this system, he provides a wide variety of large-signal measurement capabilities for model verification and for FET and IC characterization for HP internal R&D and also for an HP external power measurement business.